

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A phase locked loop circuit comprising:

 a phase control unit, a frequency control unit and an oscillator;

 a first feedback circuit loop which feeds back an output of said oscillator to said oscillator through said phase control unit which operates for integral control; and

 a second feedback circuit loop which feeds back the output of said oscillator to said oscillator through said frequency control unit which operates for proportional control,

 wherein said first feedback circuit loop and said second feedback circuit loop are connected to said oscillator at all times so as to carry out the integral control and the proportional control continuously.

Claim 2 (Currently Amended): The phase locked loop circuit as claimed in claim 1, wherein said second feedback circuit loop includes a first converter circuit for conversion of said first clock signal into a first current; a second converter circuit for conversion of said second clock signal to a second current, and a current adder circuit for adding said first current and said second current together.

Claim 3 (Previously Presented): The phase locked loop circuit as claimed in claim 1, wherein said second feedback circuit includes a first converter

circuit for conversion of said first clock signal to a first voltage, a second converter circuit for conversion of said second clock signal to a second voltage, and a voltage adder circuit for adding said first voltage and said second voltage together.

Claim 4 (Currently Amended): A phase locked loop circuit comprising:

- a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;
- a second control signal generator unit for generating based on the input signal a second control signal for proportional control of an output signal;
- an oscillator responsive to the first and second control signals for outputting a clock signal;
- a first loopfeedback circuit for feeding back an output of said oscillator to said oscillator through said first control signal generator unit; and
- a second loopfeedback circuit for feeding back the output of said oscillator to said oscillator through said second control signal generator unit,

wherein said first loopfeedback circuit and said second loopfeedback circuit are connected to said oscillator at all times so as to operate continuously.

Claim 5 (Previously Presented): The phase locked loop circuit as claimed in claim 4, wherein said first control signal generator unit uses a difference in phase between said input signal and said output signal to generate said first control signal, whereas said second control signal generator unit uses a difference in

frequency between said input signal and said output signal to generate said second control signal.

Claim 6 (Previously Presented): The phase locked loop circuit as claimed in claim 4 or 5, wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

Claim 7 (Previously Presented): The phase locked loop circuit as claimed in claim 4 or 5, wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first voltage, a second converter circuit for conversion of an output signal to a second voltage, and a voltage adder circuit for adding together said first voltage and said second voltage.

Claim 8 (Previously Presented): The phase locked loop circuit as claimed in claim 6, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits folded for connection together.

Claim 9 (Previously Presented): An information processing apparatus comprising:

a clock generator unit including a first control signal generator unit for generation of a first control signal based on a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal based on a difference in frequency between an input signal and an output signal, and an oscillator for generation of a clock signal based on said first control signal and said second control signal;

a clock control unit for controlling the clock signal as output from said clock generator unit; and

a logic unit for processing data based on the clock signal as generated by said clock generator unit.

Claim 10 (Previously Presented): The information processing apparatus as claimed in claim 9, wherein said clock control unit is operable to control the clock signal as generated from said clock generator unit on the basis of a control signal as externally supplied thereto.

Claim 11 (Previously Presented): An information processing apparatus comprising:

a clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input thereto;

a clock control unit for controlling said first clock signal as input to said clock generator unit; and

a logic unit for processing data on the basis of said second clock signal.

Claim 12 (Previously Presented): The information processing apparatus as claimed in claim 11, wherein said clock control unit controls said first clock signal on the basis of a control signal as externally supplied thereto.

Claim 13 (Original): An information processor apparatus comprising:

a clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input;

a plurality of circuits operable based on said second clock signal as output from said clock generator unit; and

an interface for transmission of said second clock signal to more than one circuit selected from among said plurality of circuits being operable with a power supply different from that of said clock generator unit.

Claim 14 (Currently-Amended): An information processing system comprising:

an information processing apparatus for data processing based on a clock frequency; and

a circuitry connected to said information processing apparatus, for outputting an internal state,

wherein said information processing apparatus renders variable ~~at~~the clock frequency based on a remaining charge of a battery so that said information processing apparatus operates on a frequency commensurate ~~which~~with the remaining charge of said battery.

Claim 15 (Previously Presented): The information processing system as claimed in claim 14, wherein said information processing apparatus includes a first control signal generator unit for generation of a first control signal from a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal from a difference in frequency between an input signal and output signal, and an oscillator for outputting a clock signal on the basis of said first control signal and said second control signal.

Claim 16 (Previously Presented): The information processing system as claimed in claim 14, wherein said information processing apparatus includes a first feedback circuit for use in generating a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal synchronized in frequency with said first clock signal as input thereto.

Claim 17 (Previously Presented): The information processing system as claimed in claim 14, 15 or 16, wherein said peripheral circuitry includes a power supply circuit, and said information processing apparatus renders variable the clock frequency on the basis of a remaining amount of said power supply circuit.

Claims 18-23 (Canceled):

Claim 24 (Previously Presented): A phase locked loop circuit

comprising:

a phase comparator circuit for outputting a phase difference signal from anyone of two output terminals in accordance with a phase difference between two signals as input thereto;

a charge pump circuit responsive to receipt of the phase difference signal from said phase comparator circuit for permitting charging and discharging of a capacitor to generate a control voltage signal; and

an oscillator responsive to the control voltage signal from said charge pump circuit for adjusting a transmission frequency, wherein said charge pump circuit includes a first current switch circuit for charging up said capacitor in deference to the phase difference signal as output from one output terminal of said phase comparator circuit, and a second current switch circuit for discharging said capacitor in response to the phase difference signal as output from a remaining one of the output terminals of said phase comparator circuit, and

wherein said first and second current switch circuits comprise a current switch using a CMOS inverter with a control electrode forward-biased and a complementary paired output voltage switch for driving said current switch with an output connected to a low voltage-side electrode of said current switch.

Claim 25 (Canceled):

Claim 26 (Previously Presented): The phase locked loop circuit as claimed in claim 7, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits connected together in a folded fashion.

Claims 27-31 (Canceled):

Claim 32 (Previously Presented): A phase locked loop circuit comprising:

- a first feedback circuit operatively responsive to receipt of a first clock signal, for generating a second clock signal synchronized in phase with the first clock signal; and
- a second feedback circuit for generation of said second clock signal substantially equal in frequency to said first clock signal as input thereto, said second feedback circuit comprising:
 - a first converter for conversion of said first clock signal into a first current;
 - a second converter for conversion of said second clock signal to a second current; and
 - an adder for adding said first current and said second current together.

Claim 33 (Previously Presented): A phase locked loop circuit

comprising:

a first feedback circuit operatively responsive to receipt of a first clock signal, for generating a second clock signal synchronized in phase with the first clock signal; and

a second feedback circuit for generation of said second clock signal substantially equal in frequency to said first clock signal as input thereto, said second feedback circuit comprising:

a first converter for conversion of said first clock signal into a first voltage;

a second converter for conversion of said second clock signal to a second voltage; and

an adder for adding said first voltage and said second voltage together.

Claim 34 (Previously Presented): A phase locked loop circuit

comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating, based on the input signal, a second control signal for proportional control of an output signal; and

an oscillator responsive to the first and second control signals, for outputting a clock signal;

wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

Claim 35 (Previously Presented): A phase locked loop circuit comprising:

a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating, based on the input signal, a second control signal for proportional control of an output signal; and

an oscillator responsive to the first and second control signals for outputting a clock signal;

wherein said first control signal generator unit uses a difference in phase between said input signal and said output signal to generate said first control signal, whereas said second control signal generator unit uses a difference in frequency between said input signal and said output signal to generate said second control signal; and

wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

Claim 36 (Previously Presented): The phase locked loop circuit as claimed in claim 34, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits folded for connection together.

Claim 37 (Previously Presented): The phase locked loop circuit as claimed in claim 35, wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits folded for connection together.

Claim 38 (Previously Presented): A phase locked loop circuit comprising:

- a first control signal generator unit responsive to receipt of an input signal, for generating a first control signal for integral control of an output signal;
- a second control signal generator unit for generating, based on the input signal, a second control signal for proportional control of an output signal; and
- an oscillator responsive to the first and second control signals, for outputting a clock signal;

wherein said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first voltage, a second converter circuit for conversion of an output signal to a second voltage, and a voltage adder circuit for adding together said first voltage and said second voltage; and

wherein said first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits connected together in a folded fashion.